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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/222,524	12/28/98	MATSUDA S	NEC-N98039

EXAMINER	
PAREKH, N	
ART UNIT	PAPER NUMBER
2811	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary

Application No.	Applicant(s)
09/222,524	Schulchl
Examiner	**Group Art Unit**
Nitin Parekh	2811

☒ Responsive to communication(s) filed on *Dec 28, 1998*

☐ This action is **FINAL.**

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire *3* month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claim

☒ Claim(s) *1-20* is/are pending in the applicat

Of the above, claim(s) _____ is/are withdrawn from consideration

☐ Claim(s) _____ is/are allowed.

☒ Claim(s) *1-20* is/are rejected.

☐ Claim(s) _____ is/are objected to.

☐ Claims _____ are subject to restriction or election requirement.

Application Papers

☐ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

☐ The proposed drawing correction, filed on _____ is ☐ approved ☐ disapproved.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

☒ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☒ All ☐ Some* ☒ None of the CERTIFIED copies of the priority documents have been

☒ received.

☐ received in Application No. (Series Code/Serial Number) _____.

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

☒ Notice of References Cited, PTO-892

☐ Information Disclosure Statement(s), PTO-1449, Paper No(s). _____

☐ Interview Summary, PTO-413

☐ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

— SEE OFFICE ACTION ON THE FOLLOWING PAGES —

DETAILED ACTION

Claim Objections

1. Claims 1, 4, 6, 11 and 16 are objected to because of the following informalities:

   A. Pages 10-13, Lines 9, 8, 8 and 8 respectively: Delete "confronting" and insert "conforming".

   B. Claim 4, line 2: Delete "ship" and insert "chip".

Appropriate correction is required.

Specification

2. Page 3, line 14: Delete "winning" and insert "wiring".

3. Page 8, line 19: Delete "confronting" and insert "conforming".

Claim Rejections - 35 USC § 103

4 The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over the admitted prior art in view of Rostoker (US Pat. 5399898), Kata et al (US Pat. 5905303) and Liang (US Pat. 5952726).

Regarding claims 1 and 11, the admitted prior art discloses a semiconductor device comprising:

- a wiring substrate/tap automated bonding (TAB) substrate/film carrier having a predetermined pattern of wiring formed on one surface and having a number of through-holes

- a semiconductor chip disposed on the other surface of the wiring substrate having chip electrodes and a wiring layer

- a number of bumps formed respectively in through-holes in conforming relationship with the chip electrodes and electrically connecting the wiring with the electrode.

The admitted prior art fails to specify the semiconductor chip having two or more chip electrodes in a common wiring layer. Rostoker teaches using a semiconductor device with a variety of internal connections where two electrodes (222 c and d in Fig. 2b) are connected to a common wiring layer (Fig. 2b; Col. 11, line 23-Col. 12, line 13) in a flip-chip assembly. Therefore, it would have been obvious to the person of ordinary skill in the art to provide two or more chip electrodes in a common wiring layer in the semiconductor chip to increase the internal connection capability using Rostoker's teaching in the admitted prior art as cited in claims 1 and 11.

Regarding claims 2 and 12, the admitted prior art fails to show an arrangement of the chip electrodes. Kata et al teach using a variety of layouts for the chip electrodes where the chip electrodes are arranged from the edge of the chip towards it's inner side (Fig. 5B, 13B and 17B; Col. 4, line 46, Col. 7, line 30 and Col. 8, line 66). Therefore, it would have been obvious to the

person of ordinary skill in the art to select an arrangement of the chip electrodes where they are arranged from an edge of the chip towards it's inner side to meet the design requirement using Kata et al's teaching in the admitted prior art as cited in claims 2 and 12.

Regarding claims 3 and 13, the admitted prior art fails to show an arrangement of the chip electrodes being parallel to an edge of the chip and the wiring being bent at least one position. Kata et al teach using a variety of layouts for the chip electrodes and the wiring where the chip electrodes are arranged parallel to an edge of the chip and the wiring is bent at various positions (Fig. 5B, 13B and 17B; Col. 3-10). The cited reference by Liang teaches using power/signal wiring layout with patterns of different dimensions, shapes where the wiring is bent at various positions (Fig. 4A; Col. 7, line 10) to meet the chip design ground rules (Fig. 1-4, Col. 3-9). Therefore, it would have been obvious to the person of ordinary skill in the art to select an arrangement of the chip electrodes where they are arranged parallel to an edge of the chip and the wiring is bent at least one position to meet the design requirement using Kata et al's teaching in the admitted prior art as cited in claims 3 and 13.

Regarding claims 4 and 14, the admitted prior art fails to specify the chip electrodes being parallel to an edge of the chip and the wiring having an end width larger than an interelectrode distance between the chip electrodes. As explained above for claims 1 and 3, Kata et al and Liang teach using a variety of arrangements and shapes/dimensions of electrode layout and wiring

patterns to meet the chip design ground rules. Therefore, it would have been obvious to the person of ordinary skill in the art to select an arrangement of the chip electrodes where they are arranged parallel to an edge of the chip and the wiring dimension which has an end width larger than an interelectrode distance between the chip electrodes to meet the design requirement using Kata et al's and Liang's teachings in the admitted prior art as cited in claims 4 and 14.

Regarding claims 5 and 15, the admitted prior art fails to specify the chip electrodes comprising at least one kind of terminal selected from ground, power-source and signal terminals of the semiconductor chip. Liang teaches using the chip electrodes comprising ground, power-source and signal terminals of the semiconductor chip in a flip-chip assembly (Fig. 4A-C; Col. 2-9; Fig. 1-7). Therefore, it would have been obvious to the person of ordinary skill in the art to incorporate the chip electrodes comprising at least one kind of terminal selected from ground, power-source and signal terminals of the semiconductor chip to meet the electrical/design requirements using Liang's design in the admitted prior art as cited in claims 5 and 15.

Claims 6 and 16 are rejected as explained above for claims 1 and 11 respectively.

Claims 7 and 17 are rejected as explained above for claims 2, 1 and 12, 11 respectively.

Claims 8 and 18 are rejected as explained above for claims 3, 1 and 13, 11 respectively.

Claims 9 and 19 are rejected as explained above for claims 4, 1 and 14, 11 respectively.

Claims 10 and 20 are rejected as explained above for claims 5, 1 and 15, 11 respectively.

Papers related to this application may be submitted directly to Art Unit 2811 by facsimile transmission. Papers should be faxed to Art Unit via Technology Center 2800 fax center located in Crystal Plaza 4, room 4C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (15 November 1989).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin Parekh whose telephone number in (703) 305-3410. The examiner can be normally reached on Monday-Friday from 08:30 am-5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas, can be reached on (703) 308-2772. The fax number for the organization where this application or proceeding is assigned is (703) 308-7722 or 7724.

Tom Thomas

Nitin Parekh

08-04-00

Tom Thomas
Supervisory Patent Examiner
Technology Center 2800